IN THE CLAIMS:

Please cancel claim 9 without prejudice to or disclaimer of the subject matter recited therein.

Please amend claims 1, 2, 6-8, and 10-12 as follows:

LISTING OF CURRENT CLAIMS

Claim 1. (Currently Amended) An output buffer with low-voltage devices to driver high-voltage signals, comprising:

a tri-state control circuit, capable of receiving and processing external low-voltage signals and high-voltage signals and outputting at least two resulting signals;

a level converter, connected to the tri-state control circuit by one end thereof, for receiving the resulting signals so as to convert low voltage swing to high-voltage swing;

an output end module, consisting of a plurality of serial-connected metal-oxide semiconductor field effect transistors;

a first taper buffer, having one end connecting to the level converter and another end thereof connecting to the output end module; and

a second taper buffer, having one end connecting to the tri-state control circuit and another end thereof connecting to the output end ~~module.~~ module, wherein the plurality of serial-connected metal-oxide semiconductor field effect transistors include at least a native Vt NMOS transistor.

Claim 2. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein the maximum voltage receivable by the ~~plural MOSFETs~~ plurality of serial-connected metal-oxide semiconductor field effect transistors is 2.5V

Claim 3. (Original) The output buffer with low-voltage devices of claim 1, wherein the output buffer is capable of driving high-voltage signals for PCI-X applications.

Claim 4. (Original) The output buffer with low-voltage devices of claim 3, wherein the output buffer is operating between 133 MHz and 66 MHz in PCI-X environment.

Claim 5. (Original) The output buffer with low-voltage devices of claim 1, wherein the output buffer is designed in a 0.13 μm 1V/2.5V CMOS process.

Claim 6. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein the tri-state output buffer consists of a CMOS NAND gate and a CMOS NOR ~~gate~~ gate.

Claim 7. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein ~~the~~ PMOS and NMOS transistors of the first taper buffer are 2.5V nominal Vt ~~transistor~~ transistors.

Claim 8. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein ~~the~~ PMOS and NMOS transistors of the second taper buffer are 1V nominal Vt transistors.

Claim 9. (Cancelled)

Claim 10. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein ~~further includes~~ the plurality of serial-connected metal-oxide semiconductor field effect transistors include at least a 1V NMOS transistor.

Claim 11. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein ~~the~~ a swing voltage of the first taper buffer is ~~1V~3.3V.~~ between 1V and 3.3V.

Claim 12. (Currently Amended) The output buffer with low-voltage devices of claim 1, wherein ~~the~~ a swing voltage of the second taper buffer is ~~0V~1V~~ between 0V and 1V.